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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/667,491	09/23/2003	Robert Sheffield	57983.000131	1242

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EXAMINER	
VAN, LUAN V	

ART UNIT	PAPER NUMBER
1753	

DATE MAILED: 03/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/667,491	SHEFFIELD ET AL.	
	Examiner	Art Unit	
	Luan V. Van	1753	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,19-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,19-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Applicant's amendment of January 19, 2006 does not render the application allowable.

Status of Objections and Rejections

All rejections from the previous office action are maintained.

New rejections under 35 U.S.C. 103(a) are necessitated by the amendments.

Election/Restrictions

The restriction requirement was made FINAL in the previous office action. Therefore, product claims 7-18 will not be considered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-6, 19 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Tanaka et al.

Regarding claim 1, Tanaka et al. teach a method for forming a bonded ceramic-metal composite substrate, the method comprising the step of: providing a layer of the circuit board 1 having the conductive circuit trace 2 (figure 1) on a surface thereof; and reducing a surface roughness (column 2 lines 23-35) of at least one surface of the conductive circuit trace on the surface of the circuit board layer. The method of Tanaka et al. would improve performance of a signal transmitted via the conductive circuit trace, since the surface roughness of the copper element 2 is reduced.

Regarding claim 2, Tanaka et al. teach wherein the step of reducing the surface roughness includes mechanical polishing the at least one surface (column 4 lines 59-64).

Regarding claims 3 -5, Tanaka et al. teach wherein the surface roughness of the at least one surface is reduced to no more than 3 μm (median surface roughness), and a maximum surface roughness of no greater than 18 μm (column 2 lines 23-35), which is within the range of the instant claims.

Regarding claim 6, Tanaka et al. teach wherein the at least one surface of the conductive circuit trace includes one of a group consisting of: a surface parallel and distal to a surface of the circuit board; a surface parallel and proximal to the surface of the circuit board; and a surface perpendicular to the surface of the circuit board (figure 1).

Regarding claim 19, Tanaka et al. teach wherein the conductive circuit trace is formed on the surface of the circuit board layer 1 (figure 1).

Regarding claim 20, Tanaka et al. teach wherein the conductive circuit trace 2 is bonded (i.e., affixed, column 3 lines 56-60) to the surface of the circuit board layer 1.

Claims 1-2, 6 and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Taylor et al. '528.

Regarding claim 1, Taylor et al. '528 teach a method for electroplating on at least one surface of the conductive circuit trace, such as conductors either 310 or 324 in figure 3, on the surface of a circuit board 304. The method of Taylor et al. '528 would improve the performance of signal transmitted trace via a conductive circuit by reducing surface roughness, since a uniform layer of metal (either 324 or 326) is being electrodeposited (example 1), and since the method of Taylor et al. '528 is the same as that of the instant claim, i.e., electroplating.

Regarding claim 2, Taylor et al. '528 teach reducing the surface roughness includes electropolishing (i.e. anodic pulses) at least one surface in which "the anodic pulses should be relatively short in order to favor removal of excess metal from the convex and peak portions of the substrate surface" (column 8 lines 63-67); and electroplating (i.e. cathodic pulses) at least one surface. In addition, Taylor et al. '528 teach "Although the anodic removal of excess metal reduces the overall efficiency of the electroplating process, the benefits of obtaining a uniform coating over the surface and the through-holes provides a benefit to the manufacturing process" (column 9 lines 8-12).

Regarding claim 6, Taylor et al. '528 teach at least one surface the conductive circuit trace includes a surface parallel and distal surface circuit board (conductor 310); and a surface perpendicular to the circuit board (conductor 328). In addition, Taylor et al. '528 teach "A uniform layer 326 of copper has been deposited over the first layer 324 and onto the inner surface 322 of the through-hole 320" (column 10 lines 49-52).

Regarding claim 19, Taylor et al. '528 teach the conductive circuit trace 312 is formed on the surface of the circuit board layer 304.

Claims 1-2, 6 and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Ozeki et al.

Regarding claim 1, Ozeki et al. teach a method for electroplating (paragraph 52) on at least one surface of the conductive circuit trace, such as circuit pattern 22 in figure 1, on the surface of a circuit board 20. The method of Ozeki et al. would improve the performance of signal transmitted trace via a conductive circuit by reducing the surface roughness, and since the method of Ozeki et al. is the same as that of the instant claim, i.e., electroplating.

Regarding claim 2, Ozeki et al. teach reducing the surface roughness includes electroplating at least one surface (paragraph 52).

Regarding claim 6, Ozeki et al. teach at least one surface the conductive circuit trace includes a surface parallel and distal surface circuit board, such as circuit pattern 22 in figure 1.

Regarding claim 19, Ozeki et al. teach the conductive circuit trace 312 is formed on the surface of the circuit board layer 304.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 3-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Taylor et al. '528 in view of Nagai et al. or Taylor '231.

Taylor et al. '528 teach the method as described above in addressing claim 1. Taylor et al. '528 also teach that an appropriate plating bath including additives can be selected to improve the uniformity of the deposited coating (column 9 lines 50-60).

The difference between the reference to Taylor et al. '528 and the instant claims is that the reference does not explicitly teach the specific value of the surface roughness of the conductive trace.

Nagai et al. teach "Large surface roughness of a copper foil results in the skin effect such that the current of electric signal having 1 GHz or more of frequency locally flows only on the surface of a coil. As a result, the impedance increases and the transmission of high-frequency signals is seriously influenced. Fine surface roughness is, therefore, necessary for conductive material used in a high-frequency circuit. The present inventors examined the relationship between the surface roughness and the high-frequency performance and discovered that 2 micrometer or less of surface roughness in terms of the terms of the ten-point average surface-roughness (Rz) attains the desired high-frequency performance. The fine roughness can be provided by means of producing a wrought copper foil or electro-deposited copper foil under appropriate conditions, or chemically or electrolytically polishing the surface of a copper foil" (paragraph 28).

Taylor '231 teaches a method for electropolishing a metal surface to reduce its roughness, and that a "smooth polished surface suitable for high-quality commercial product might have an Ra value defined by the end use, in the order of for example 5 μm or less" (column 3 lines 36-43).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method of Taylor et al. '528 by electroplating or electropolishing a conductive trace to have a surface roughness of less than a few

micrometer as taught by either Nagai et al. or Taylor '231, because it would decrease the resistivity and impedance of a high-frequency signal.

Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Taylor et al. '528 in view of Lin et al.

Taylor et al. '528 teach the method as described above in addressing claim 1. Taylor et al. '528 differs from the instant claims in that the reference does not explicitly teach affixing the conductive circuit trace to the surface.

Lin et al. teach a method for attaching conductive traces to plural, stacked, encapsulated semiconductor die using a removable transfer film. A pattern of conductive traces is formed on a film of transfer material. The conductive traces are attached to a die and the film of transfer material is then peeled from the pattern of conductive traces (abstract).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified the method of Taylor et al. '528 by affixing the conductive traces as taught by Lin et al., because it would be a low cost manufacturing method compared to traditional additive thin-film processing (column 1 lines 45-51).

Claims 3-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ozeki et al. in view of Nagai et al. or Taylor '231.

Ozeki et al. teach the method as described above in addressing claim 1.

The difference between the reference to Ozeki et al. and the instant claims is that the reference does not explicitly teach the specific value of the surface roughness of the conductive trace.

Nagai et al. teach "Large surface roughness of a copper foil results in the skin effect such that the current of electric signal having 1 GHz or more of frequency locally flows only on the surface of a coil. As a result, the impedance increases and the transmission of high-frequency signals is seriously influenced. Fine surface roughness is, therefore, necessary for conductive material used in a high-frequency circuit. The present inventors examined the relationship between the surface roughness and the high-frequency performance and discovered that 2 micrometer or less of surface roughness in terms of the terms of the ten-point average surface-roughness (Rz) attains the desired high-frequency performance. The fine roughness can be provided by means of producing a wrought copper foil or electro-deposited copper foil under appropriate conditions, or chemically or electrolytically polishing the surface of a copper foil" (paragraph 28).

Taylor '231 teaches a method for electropolishing a metal surface to reduce its roughness, and that a "smooth polished surface suitable for high-quality commercial product might have an Ra value defined by the end use, in the order of for example 5 μm or less" (column 3 lines 36-43).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method of Ozeki et al. by electroplating or

electropolishing a conductive trace to have a surface roughness of less than a few micrometer as taught by either Nagai et al. or Taylor '231, because it would decrease the resistivity and impedance of a high-frequency signal.

Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ozeki et al. in view of Lin et al.

Ozeki et al. teach the method as described above in addressing claim 1. Ozeki et al. differs from the instant claims in that the reference does not explicitly teach affixing the conductive circuit trace to the surface.

Lin et al. teach a method for attaching conductive traces to plural, stacked, encapsulated semiconductor die using a removable transfer film. A pattern of conductive traces is formed on a film of transfer material. The conductive traces are attached to a die and the film of transfer material is then peeled from the pattern of conductive traces (abstract).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified the method of Ozeki et al. by affixing the conductive traces as taught by Lin et al., because it would be a low cost manufacturing method compared to traditional additive thin-film processing (column 1 lines 45-51).

Response to Arguments

Applicant's arguments filed January 19, 2006 have been fully considered but they are not persuasive.

It is noted that the claims presented encompass a very broad scope. As such, the claims are open to a very broad interpretation.

In the arguments presented on page 5 of the amendment, the applicant suggests that the references do not disclose every limitation of the rejected claim, specifically that the references do not teach providing a conductive circuit trace on the surface of the circuit board and reducing the surface roughness of the conductive circuit trace. The examiner respectfully disagrees. As presented above, Taylor et al. '528 teach a method for electroplating on at least one surface of the conductive circuit trace, such as conductors either 310 or 324 in figure 3, on the surface of a circuit board 304. The method of Taylor et al. '528 would improve the performance of signal transmitted trace via a conductive circuit by reducing surface roughness, since the method of Taylor et al. '528 is the same as that of the instant claim, i.e., electroplating. Likewise, Ozeki et al. teach a method for electroplating (paragraph 52) on at least one surface of the conductive circuit trace, such as circuit pattern 22 in figure 1, on the surface of circuit board 20. The method of Ozeki et al. would improve the performance of signal transmitted trace via a conductive circuit by reducing the surface roughness, since the method of Ozeki et al. is the same as that of the instant claim, i.e., electroplating. Additionally, with respect to the process of reducing the surface roughness, the mere recognition of latent properties or additional advantages present in the prior art does not

render nonobvious an otherwise known invention; and the discovery of an unknown but inherent function of the prior art cannot be used as the basis for patentability when the differences between the prior art and the instant invention would otherwise be obvious. (MPEP 2145).

Therefore, these references anticipate the independent claim.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luan V. Van whose telephone number is 571-272-8521. The examiner can normally be reached on M-F 9:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nam Nguyen can be reached on 571-272-1342. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LVV
2/28/2006

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